

Implementation and integration of a systematic DBPM calibration with PLL frequency synthesis and FPGA*

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Beam current dependence resulted from nonlinearity and asymmetry of the four channels of digital BPM (Beam Position Monitor) processor deteriorates the BPM performance. A systematic solution based on signal source calibration tactics has been carried out to rectify this defect. It is optimized for implementation in FPGA. Mathematical illustrations of the calibration method, hardware and software design and implementation are presented. A signal source circuit using frequency synthesis technique is designed as calibration standard. Data acquisition system using JAVA web technology and Ethernet is introduced. Integrated FPGA implementation code architecture is presented, and experimental test results show that the method implemented in FPGA is feasible. Compared to other methods, our approach can rectify the nonlinearity and asymmetry simultaneously. The whole solution is integrated into the DBPM processor and can be executed online.

Keywords: Digital Beam Position Monitor (DBPM), Beam current dependence calibration, Frequency synthesis RF circuit, numerical interpolation method, FPGA, Ethernet Java Web data acquisition

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I. INTRODUCTION

Beam Position Monitor (BPM) is a critical instrument for supervisory control of accelerator performance [1]. The digital BPM processor (DBPM) [2, 3] developed in our lab [4] with a software defined radio architecture [5] moves most of the signal processing module to FPGA and use the common difference over sum ratio method to calculate the beam position [6], as shown in Fig. 1.

However, like other BPM processors, four identical channels are requisite parts. Their asymmetry and nonlinearity can deteriorate the measurement of beam position. A typical problem of this kind is the beam current dependence. As shown in Fig. 2, although the actual beam position remains the same, the measured position depends on the beam current deviates from its true position. The weaker the beam current is, the worse the deviation will be.

Various calibration methods have been used [7–9] to solve this type of problem, but methods like channel switching would cause switching noise which will impair resolution of the wide-band beam position information (turn by turn, for example).

In our solution, rectification on each channel is carried out a standard signal source as a common reference, which is done after the digital signal processor (DSP) module in the frequency domain. Compared to other methods [7–9], our approach rectifies the nonlinearity and asymmetry simultaneously. We have optimized the method for easy implementation in FPGA. The whole calibration is integrated into DBPM processor.

II. METHODS

A. Illustration of calibration method

To simplify the problem by considering just two channels, the ideal position is calculated by Eq. (1):

$$\text{position} = \frac{A - B}{A + B}, \quad (1)$$

where, A and B are the respective original signal level of the pickup at each channel.

Nevertheless, practical beam positions are obtained by calculations after signal processing module on the RF board (Fig. 1), thus the measured position shall be described in Eq. (2):

$$\text{uncalibrated - position} = \frac{a_G(A) - b_G(B)}{a_G(A) + b_G(B)}, \quad (2)$$

where a_G and b_G are the transfer function or response curve of the RF front end of channel A and B, respectively, and A and B are corresponding original signal at the pickup before follow-up processing.

Ideally, both the crude positions at the pickup and the calculated position at the end of processor depend only on the beam position, which is the goal of position monitoring, but beam current dependence problems occur in real world situation.

Practically, due to inconsistency and nonlinearity of the analog electronic device, the transfer function of the four channels of DBPM tends to behave differently and heads to have distinct outputs from the same input. As shown in Fig. 3(a), with the same inputs, the outputs of four channels are not consistent. And nonlinearity means at different input power levels, the gain of the channel is not consistent, in other

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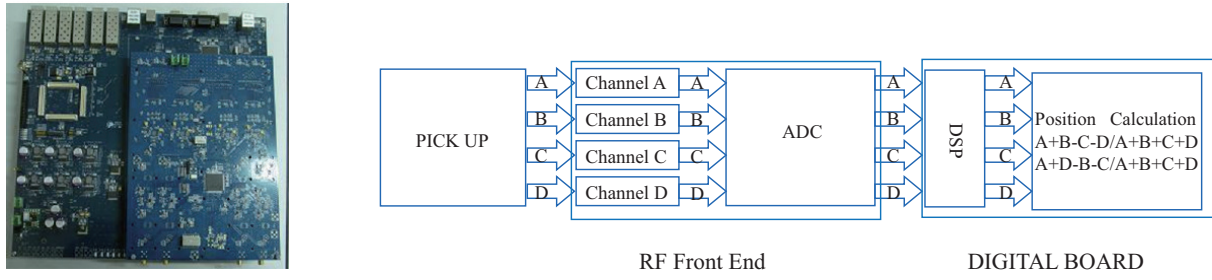


Fig. 1. (Color online) Simplified DBPM architecture. Left: BPM prototype. Right: Simplified DBPM architecture.

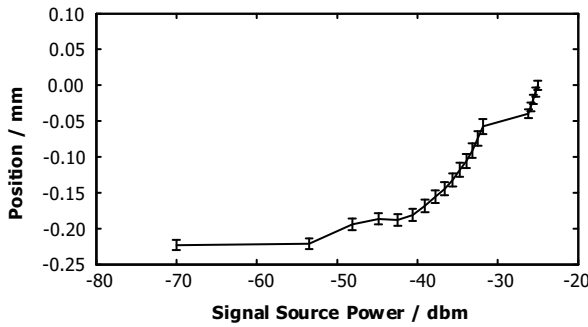


Fig. 2. Beam current dependence in position measurement.

words, a non-linear gain. As shown in Fig. 3(b), the third order term magnitude is almost 40 times bigger than linear term.

Thus the measured position is blurred by the asymmetry and nonlinearity of respective channels.

Suppose the signal at the processor end is a function of both the beam current and position, one has

$$\begin{aligned} \text{calculated - position} &= \frac{A_m(P, I) - B_m(P, I)}{A_m(P, I) + B_m(P, I)} \\ &= C(P) + \sigma_\alpha c_\alpha I^\alpha, \end{aligned} \quad (3)$$

where, the first term depends solely on position, the second term is beam dependence factor.

The orbit stability shall become worse for a third generation of synchrotron radiation facility if this issue is poorly resolved.

The calibration is aimed at wiping off this dependence term.

$$\text{calibrated - position} = \frac{a_c[a_G(A)] - b_c[b_G(B)]}{a_c[a_G(A)] + b_c[b_G(B)]}, \quad (4)$$

where, a_c and b_c rectify the corresponding channel to a common ideal channel. By taking a_c and b_c as the reverse of a_G and b_G , the gain inconsistency and nonlinearity across the channels will be eliminated, in other words, the accuracy of measured position will not be affected by the gain inconsistency and nonlinearity, as shown in Eq. (5):

$$\begin{aligned} \text{calibrated - position} &= \frac{a_c[a_G(A)] - b_c[b_G(B)]}{a_c[a_G(A)] + b_c[b_G(B)]} \\ &= \frac{a_G^{-1}[a_G(A)] - b_G^{-1}[b_G(B)]}{a_G^{-1}[a_G(A)] + b_G^{-1}[b_G(B)]} \\ &= \frac{A - B}{A + B}. \end{aligned} \quad (5)$$

B. Interpolation approximation to the amplitude response curve

To use Eq. (5), the mathematical expression of a_c and b_c or equivalently a_G and b_G should be known.

In our approach, discrete points of the response curve a_G and b_G are taken down as control points for interpolation to approximate the response curve.

If several discrete points of a curve are known to approximate the original curve, a general expression of interpolation to approximate this curve [10] with n control points shall be

$$I_h(x) = \sum_j f_j l_j(x), \quad (6)$$

where, $l_j(x)$ is the j^{th} blending function decided by the nearby control points, f_j is the response variable of the corresponding excitation variable x , and $I_h(x)$ is a hybrid of the blending function with weights f_j approximating the original curve.

The next task is to choose a good interpolation blending function $l_j(x)$. Speculated from a zoomed view of Fig. 3, a sole global linear approximation to each channel would poorly represent the behavior of each channel upon different input power level, but at local viscosity, a linear approximation would be good enough to depict the behaviour. Thus, the piece-wise linear interpolation method can approximate the global behavior of four channels. The whole response curve is divided into several pieces, and a piece can be approximated by Eq. (7):

$$\begin{aligned} I_{\text{local}}(x) &= \frac{x_p - x}{x_p - x_n} f_n + \frac{x - x_n}{x_p - x_n} f_p, \\ &(x_n \leq x \leq x_p), \end{aligned} \quad (7)$$

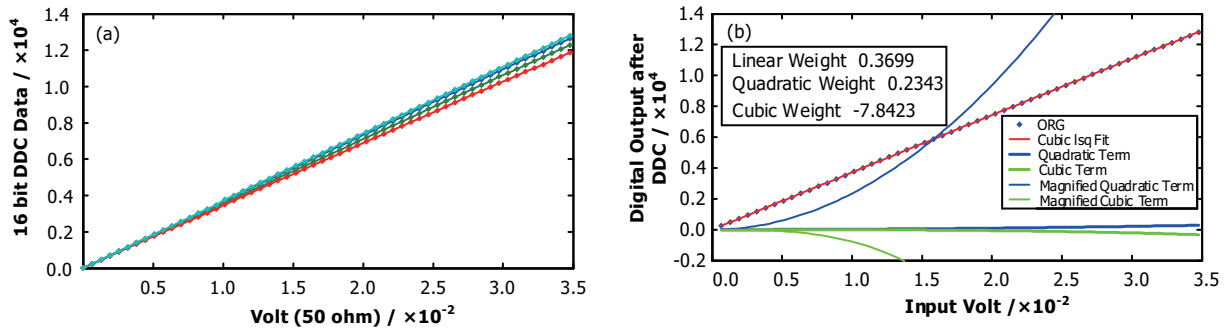


Fig. 3. (Color online) Asymmetry and nonlinearity of four channels. (a) Asymmetry of four channels. (b) Nonlinearities of four channels.

where, the blending functions are $(x_p - x)/(x_p - x_n)$ and $(x_p - x_n)/(x_p - x_n)$, (x_p, f_p) and (x_n, f_n) are control points of the piece. Fig. 4 is the graphical illustration of linear blending function for the piece. The blending function is determined by the two control points (x_p, f_p) and (x_n, f_n) . And the interpolation line mixes the two blending functions with weights f_n and f_p .

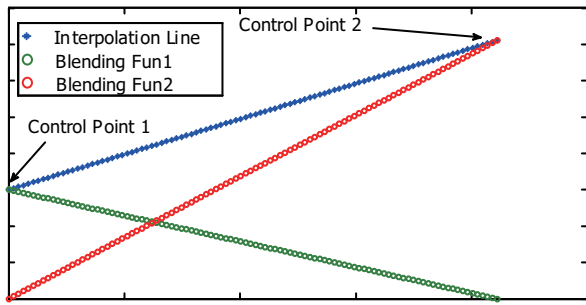


Fig. 4. (Color online) Local blending function for interpolation.

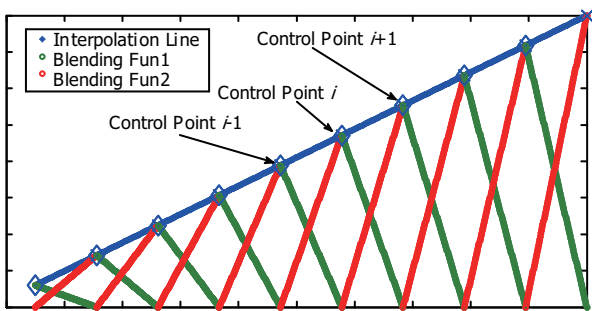


Fig. 5. (Color online) Global blending function for interpolation.

If the dynamic range is divided into m pieces, there will be a global interpolation function to approximate the response curve, as shown in Fig. 5.

The advantage of this approach is that it can be easily implemented in parallel in FPGA. The control points can be obtained online and stored in FPGA or FLASH memory. No further parameters are needed.

III. SIGNAL SOURCE CIRCUIT DESIGN AND FREQUENCY SYNTHESIS CRITERION

The interpolation method in Sec.I depends on the discrete points of the response curve. These discrete points should be taken as control points. This is done by using a standard signal source with programmable output power to traverse the dynamic range of the RF board and to record output of each channel at different levels of input power. In Fig. 3, each curve represents the gain of an RF channel at different level of input power at the same frequency.

A frequency synthesis circuit is designed on a separate board for performance evaluation of calibration solution. It is also integrated on the DBPM to provide the calibration standard reference.

As shown in Fig. 6, embedded IOCs of ARM, FPGA and CPLD are used to configure the frequency synthesis circuit to generate the desired input to the RF board of DBPM instrument. A band pass filter is used to pick out the interested harmonics from the oscillation, assisted by a hybrid of low pass filter and RF amplification. A digital controllable attenuation module is used to make the signal source and traverse the dynamic range of the RF board of BPM processor. The attenuation is controlled by CPLD, which can also be ultimately configured by ARM.

A PLL frequency synthesis scheme is used. As a feedback loop [11], PLL has prominent performance and high frequency accuracy. Integrated circuit AD4360 from ADI company is chosen as the frequency synthesis module. It has a three wire interface for crucial parameter programming. A 20 MHz XTL is fed into the chip. With external inductors, the internal VCO of AD4360 is configured to oscillate at a central frequency of 507 MHz using Eq. (8):

$$f_{\text{center}} = \frac{1}{2\pi \times \sqrt{6.2pF \times (0.9 \text{ nH} + L_{\text{ext}})}}. \quad (8)$$

The external inductor L_{ext} is set at 15 nH, and nearly 500 MHz output is in the range [12].

A dual modulus pre-scaler with charge pump approach [12] is used to get enough frequency resolution (Fig. 7). For example, to generate a frequency of 499.65 MHz with XTL oscillates at a frequency of 20 MHz, a 0.01 MHz resolution or PFD frequency can be chosen, and the R divider should be

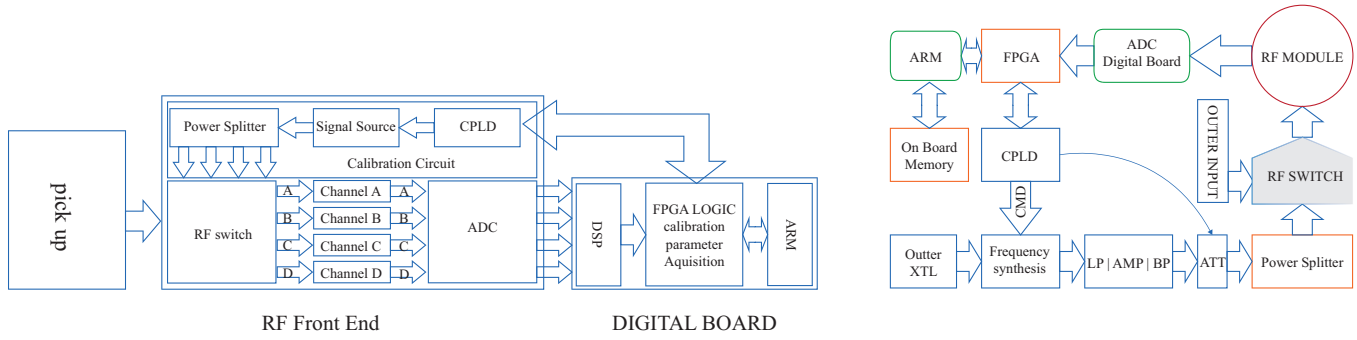


Fig. 6. Overall architecture of the calibration hardware.

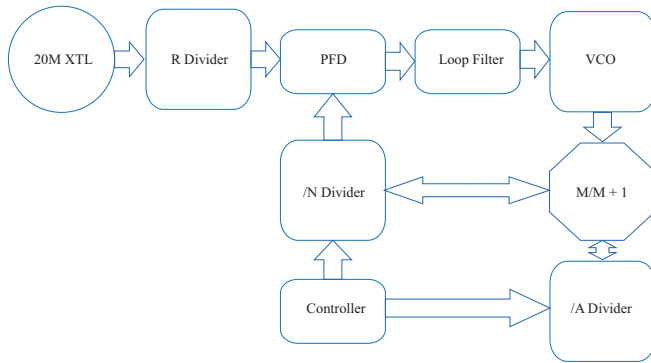


Fig. 7. Dual modulus prescaler frequency generator and critical parameters.

TABLE 1. Critical PLL synthesis parameters

XTL	20 MHz
PFD frequency (frequency resolution)	2000 counts
Total counts	49965
Prescaler	16/17
A	3122
B	13
VCO	507 MHz

programmed at 2000 (less than 14 bit). Therefore, the total integer counts needed is 49 965. So, if the pre-scaler is configured at 16/17, N should be set to 3122 (less than 13 bit) and A should be set at 13. The critical PLL synthesis parameters are shown in Table 1.

All the parameters can be dynamically programmed by ARM through CPLD for easy tuning and optimization (Fig. 6).

IV. IMPLEMENTATION IN FPGA

FPGA is widely used in digital systems for its flexibility and extensibility in digital signal processing [14]. In this solution, we use FPGA as the signal processing module and the control logic module.

Using the calibration method proposed in Secs.I and II, it is essential to take down the responses of the four channels at different input power levels as the calibrating reference points during the calibration state and calculate the reverse function in normal state. All the processes are controlled by FPGA.

A. Control logic and data flow in FPGA

A global state machine is realized in FPGA with three modes which are the configure mode, calibration mode and normal mode. Fig. 8 displays the general operation diagram of calibration logic and data flow. As the power is switched on, FPGA is initiated in the configure mode. During this stage, ARM transmits configuration parameters to FPGA through ARM interface logic in FPGA like the attenuation series, which decides whether to calibrate or not. The FPGA goes into the calibration mode or the normal mode directly. In the calibration mode, the FPGA conduct a finite state machine to traverse the dynamic range of frequency synthesis (signal source) circuit output power level. This is done by setting the digital attenuators in frequency synthesis circuit, with options of 0.5 db, 1 db, 2 db, 4 db, 8 db and 16 db, which can be combined to generate arbitrary attenuation level with a 0.5 db step. Two attenuators are cascaded such that the dynamic range of DBPM instrument can be covered.

At each attenuation, the response power levels along with the input power of the DBPM instrument are recorded in the FPGA block RAM (the parameters can be set directly by ARM in configure mode, too). After all the attenuations are traversed, the calibration parameters are stored and ready for calibration calculation.

Finally the FPGA goes into the normal mode for beam position measurement. ADC data are manipulated in the DDC module and then fed into rectification module where the calibration parameters stored during the reverse-interpolated signal source value.

During normal mode, FPGA can be forced to go to calibration mode or configure mode by ARM command. The state machine diagram of the control logic is shown in Fig. 9.

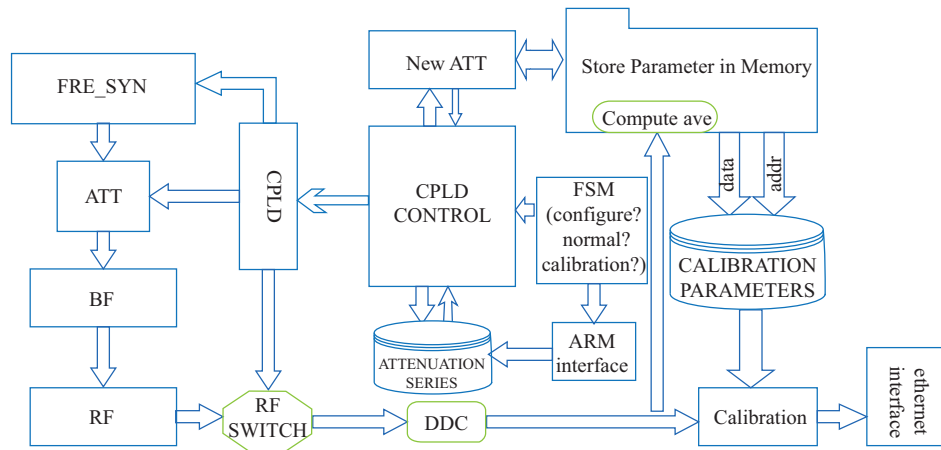


Fig. 8. Operation diagram of calibration logic and hardware circuit.

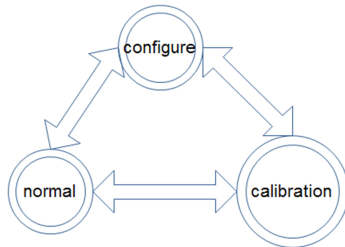


Fig. 9. Modes of the FPGA and transitions between modes.

B. Calibration dataflow inside FPGA

The calibration calculation module is after the DSP module in FPGA. The process is paralleled. In the first cascade, a segmentation module is installed for deciding the piece of current data. This is done by comparing the calibration data stored in the block RAM of FPGA. Consecutively, the controls points of this piece together with the current data are fed to the interpolation calculation module which does the computation of Eq. (6). Fig. 10 shows a brief view of the process.

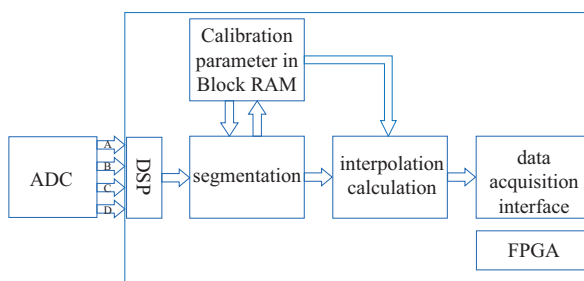


Fig. 10. Parameter acquisition and calibration calculation inside FPGA.

V. EVALUATION EXPERIMENTS AND RESULTS

A. Evaluation method and hardware setup

To testify the method's feasibility, testing hardware and data acquisition system are developed and evaluation of the method is carried out in two stages.

Firstly the FPGA is set to the calibration mode. Calibration parameters are stored in the FPGA block ram. The architecture shown in Fig. 11 is used to assess the performance of calibration scheme.

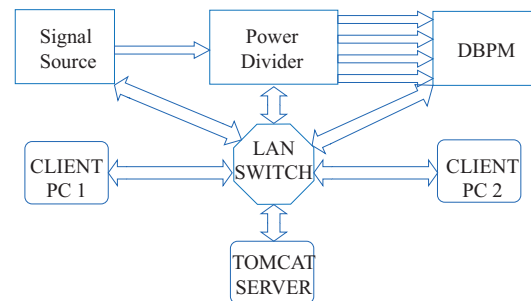


Fig. 11. Evaluation hardware setup and LAN data acquisition system.

To emulate the central beam signal, a commercial signal source is tuned at 499.6 MHz and is fed to a power divider which can generate four almost identical signals and input to the four channels of DBPM processors.

After calibration, the experimental data are obtained through the Ethernet interface of the DBPM processor and transmitted to TOMCAT SERVER and distributed to client PC through web browser like IE or Firefox.

B. Data acquisition system

LAN-PC aided data acquisition system is developed with JAVA web technology. The Schwarz signal source is remotely

controlled by the Tomcat server Machine to traverse the dynamic range of DBPM input and client PCs of the LAN can capture the data for the position calculation. After the signal source is ready, the Java Web server tells the DBPM to send packets through the Ethernet interface to server. Client PCs captures the data through server. This is shown in Fig. 12.

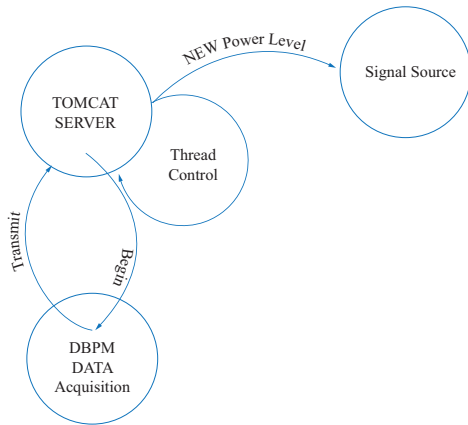


Fig. 12. (Color online) Data acquisition tread control using JAVA technology.

C. Results

Figure 13 is the comparison before and after calibration. Since the inputs to the channels of DBPM processors are approximately identical, the right position calculation result should be zero corresponding to the centered beam situation.

Without calibration, the position calculation results vary with the input power level. When the input power level is high, the position calculation is approximately zero. With an attenuated input power level, however, the position calculation

tion digresses far away from zero. This is a typical problem of beam current dependence.

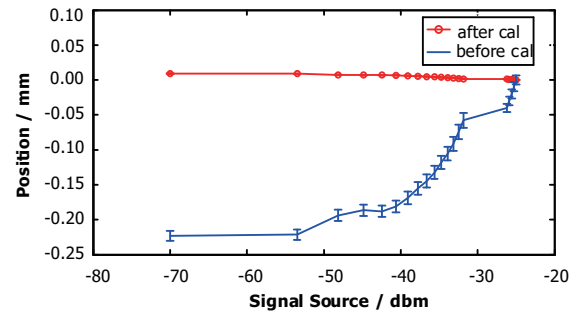


Fig. 13. (Color online) Comparison of the calculated positions before and after calibration.

With calibration, the calculated position fluctuates around zero at all levels of the input power.

From the experiments, it can be speculated that our calibration tactic rectify the beam current dependence problem quite well.

VI. CONCLUSION

The problem of beam current dependence of BPM processors is solved by the calibration method we proposed. The experimental results testify feasibility of the method. Compared to a similar calibration method implemented on PC [15], FPGA provides an equally well result and is well integrated into DBPM processor and the calibration is carried on line. Overall, this solution gives a satisfying result.

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